UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.   : 6,873,564 B2
APPLICATION NO. : 10/779425
DATED   : March 29, 2005
INVENTOR(S)   : Frankie F. Roohparvar

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On column 1, line 47, delete "modem" and insert therefor --modern--.

On column 8 line 8 delete Table 1 in its entirety and insert therefor:

TABLE 1

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0	0-1	0-1
			0	1-0	1-0
			1		
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-0-3-2	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page 256	n = A0-A7 (location 0-255)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4 ... Cn − 1, Cn ...	Not supported

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On columns 9 and 10 line 33, delete Truth Table 2 in its entirety and insert therefor:

TRUTH TABLE 2

Flash Memory Command Sequences

Operation	1st CYCLE					2nd CYCLE					3rd CYCLE				
	CMD	ADDR	ADDR	DQ	RP#	CMD	ADDR	ADDR	DQ	RP#	CMD	ADDR	ADDR	DQ	RP#
READ DEVICE Config	LCR	90H	Bank	X	H	ACTIVE	Row	Bank	X	H	READ	CA	Bank	X	H
READ Status Register	LCR	70H	X	X	H	ACTIVE	X	X	X	H	READ	X	X	X	H
CLEAR Status Register	LCR	50H	X	X	H										
ERASE SETUP/ Confirm	LCR	20H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	D0H	H/V$_{HH}$
WRITE SETUP/ WRITE	LCR	40H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	Col	Bank	DIN	H/V$_{HH}$
Protect BLOCK/ Confirm	LCR	60H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	01H	H/V$_{HH}$
Protect DEVICE/ Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	F1H	V$_{HH}$
Unprotect BLOCKS/ Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	D0H	H/V$_{HH}$
ERASE NV mode Register	LCR	30H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	C0H	H
WRITE NV mode Register	LCR	A0H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	X	H

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 22, Line 37, delete "After ERASE CONFIRM (DOH) is" and insert --After ERASE CONFIRM (D0H) is--

Column 24, Line 64, delete "A deep power-down mode is enable by" and insert --A deep power-down mode is enabled by--

Column 26, Line 15, delete "memory determines if nil blocks should" and insert --memory determines if all blocks should--

Signed and Sealed this

Twenty-sixth Day of February, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office